intervening claims. Applicant respectfully submits that the presently pending claims 5-8 are already in conditions for allowance. Reconsideration and withdrawal of the Examiner's rejection are earnestly requested.

**Summary of Applicant's Invention**

The Applicant's invention is directed to a method for erasing a non-volatile memory, wherein positive biases are applied to the drain region and the gate conductive layer, respectively, while the source region and the substrate are grounded to generate and inject hot electron holes into the charge-trapping layer.

**Response to 35 U.S.C. 103 (a) rejection**

*Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Trudel et al. (US patent no. 4,353,083, Trudel hereinafter).*

Applicant respectfully asserts that Trudel is legally deficient for the purpose of rendering claim 5 unpatentable for at least the reason that not every element of the claim was taught or suggested by Trudel such that the invention as a whole would have been obvious to one of ordinary skill in the art. The present invention specifically teaches "*applying a first positive bias to the drain region, applying a second positive bias to the gate conductive layer, and grounding the source region and the substrate to generate hot electron holes in a channel region, wherein the hot electron holes are injected into the charge-trapping layer through the nitride tunneling layer*". The technical significant of the foregoing limitations is that the biases applied can be lower than those adopted for erasing a SONOS memory having a same size as the non-volatile

memory with the nitride tunneling layer. Contrary to the Office's assertion, Trudel does not disclose applying a positive bias to the drain region. Trudel, instead, teaches applying a high voltage (+18V) to the gate, and with the source, drain and substrate grounded (col. 2, lines 33-35). Further, the erase mechanism adopted by Trudel is to apply a high voltage to the gate to eject electrons from the dielectric layer, whereas the present invention teaches applying low biases (2 to 5 volt) to both the gate and the drain to inject electron holes into the charge trapping layer. Therefore, Trudel neither suggests nor discloses the claimed invention.

For at least the foregoing reasons, claim 5 is respectfully submitted to be patentable over the prior art of record. Accordingly, the Applicant respectfully requests that the rejection under 35 USC 103(a) be withdrawn.

## CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 5-8 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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Belinda Lee
Registration No. 46,863

J.C. Patents
4 Venture, suite 250
Irvine, CA 92618
Tel.: (949) 660-0761
Fax : (949) 660-0809